



US 20210097449A1

(19) **United States**

(12) **Patent Application Publication**
Chattopadhyay et al.

(10) **Pub. No.: US 2021/0097449 A1**

(43) **Pub. Date: Apr. 1, 2021**

(54) **MEMORY-EFFICIENT SYSTEM FOR
DECISION TREE MACHINE LEARNING**

(52) **U.S. Cl.**

CPC **G06N 20/20** (2019.01); **G06N 5/04**
(2013.01); **G06N 5/003** (2013.01)

(71) Applicant: **Intel Corporation**, Santa Clara, CA
(US)

(57)

ABSTRACT

(72) Inventors: **Rita Chattopadhyay**, Chandler, AZ
(US); **Rajesh Bansal**, Sengkang (SG)

In one embodiment, a processing device for training a decision tree model includes memory and processing circuitry. The processing circuitry allocates a tree node array in memory, where the number of array elements in the tree node array equals the number of data samples in a training dataset. The processing circuitry also obtains the training dataset, which contains data samples captured at least partially by sensor(s). The processing circuitry then trains the decision tree model. For example, a root node is initially assigned to the data samples in the training dataset. The root node is recursively split into child nodes based on identified branch conditions, where each child node is assigned to a subset of data samples. The tree node array is continuously updated during training to identify the child nodes assigned to the data samples. The processing circuitry then stores the trained decision tree model in memory.

(73) Assignee: **Intel Corporation**, Santa Clara, CA
(US)

(21) Appl. No.: **17/120,059**

(22) Filed: **Dec. 11, 2020**

Publication Classification

(51) **Int. Cl.**

G06N 20/20 (2006.01)

G06N 5/00 (2006.01)

G06N 5/04 (2006.01)

100

